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AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions and listings of claims in the application:

1. (Previously presented) A processor, comprising:

a physical register file populated by a number of registers;

an instruction decoder;

a register alias table coupled to the instruction decoder;

an active list populated by a number of entries, the entries include an old field and a new field;

a free list of unallocated physical registers reclaimed from said active list; and

a misprediction condition wherein said free list reclaims mispredicted allocated said physical registers from said new field.

2. (Previously Presented) The processor of claim 1, further comprising an instruction window buffer to store dispatched instructions.

3. (Previously Presented) The processor of claim 2, wherein said dispatched instructions correlate to evicted allocated physical registers, said free list is to reclaim said evicted physical registers when said dispatched instructions retire.

4. (Previously Presented) The processor of claim 1, wherein said instruction is to write to said allocated physical register.

5. (Previously Presented) The processor of claim 1, wherein said allocated physical register is to be allocated from said free list.

6. (Cancelled)

7. (Original) The processor of claims 1, further comprising a bit field within said active list, said bit field comprising at least one bit to indicate whether the instruction is retired correctly.

8. (Previously Presented) A method for recovering registers in a processor, comprising:

detecting an exception correlating to an instruction associated with an entry on an active list;

moving a pointer on said active list to an old field and a new field after said entry; and

reclaiming during a misprediction condition allocated physical registers in said new field to a free list.

9. (Previously Presented) The method of claim 8, further comprising flushing instructions in an instruction window buffer after said instruction associated with a misprediction condition.

10. (Original) The method of claim 9, further comprising overwriting entries in said active list.

11. (Original) The method of claim 8, further comprising allocating unallocated physical registers from said free list to a register alias table.

12. (Original) The method of claim 11, further comprising moving evicted physical registers from said register alias table to said active list.

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (Previously Presented) A register renaming apparatus within a processor, comprising:

a register alias table;

a first set of registers to be renamed by said register alias table;

an active list having an old field and a new field that correlate to said registers; and

a free list comprising a second set of registers reclaimed from said active list; and a misprediction condition wherein said free list is to reclaim mispredicted allocated said registers from said new field.

20. (Previously Presented) The apparatus of claim 19, wherein said first set of registers correlate to non-retired instructions.

21. (Original) The apparatus of claim 19, wherein said active list includes a bit field.

22. (Original) The apparatus of claim 19, further comprising a pointer for said active list.